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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/718,850	11/22/2000	Ramachandra Divakaruni	BUR9-2000-0016-US1	3171

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EXAMINER
GEBREMARIAM, SAMUEL A

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/22/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/718,850	DIVAKARUNI ET AL.	
	Examiner	Art Unit	
	Samuel A Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of group I, claims 1-17 drawn to a method of making a semiconductor device in Paper No. 7 is acknowledged.

Drawings

2. Applicant's formal new drawing in Paper No. 6 is acknowledged.

Specification

3. The disclosure is objected to because of the following informalities:

page 7, line 7 refers to an implant dose of "1x1016cm-2". It appears like there is a typo. Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claims 5, 10 and 16 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Implanting impurities into the insulator will not serve any purpose as far as creating collector diffusion region in the insulator.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, are rejected under 35 U.S.C. 103(a) as being unpatentable over Horie US patent No. 5,406,113 in view of Zhao et al. US patent No. 6,037,664.

Regarding claim 1, Horie teaches a method of forming an emitter in a vertical bipolar transistor comprising: providing a substrate 14 having a collector layer 18 and a base layer 26 over the collector layer; forming a patterned mask over the collector and filling opening in the mask with emitter material (3a-3g).

Horie does not explicitly teach forming a patterned mask over the collector, filling the openings using damascene process and does not explicitly teach filling more than one opening.

Zhao teaches the use of damascene process for forming inter-connect structure in dielectric layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the damascene process taught by Zhao in to the process of Horie in order to form the emitter of the bipolar transistor since damascene process provides process simplification by reducing process steps required to form vias (column 1, lines 27-45). It would also have been obvious to one of ordinary skill in the art at the time the invention was made to make more than one opening and filling the openings in the mask with emitter material since the formation integrated circuit involves the fabrication of more than one bipolar transistor.

Regarding claim 2, Horie teaches substantially the entire process step of claim 1 above including the substrate includes an insulator layer 12 between the bottom silicon layer 10 and a top silicon layer 18, the method further comprising implanting a first impurity to form the collector layer 20 in a lower portion of the top silicon layer adjacent the insulator layer and implanting a second impurity to form the base layer in an upper portion of the top silicon layer (figs. 3a-3g).

Claims 3 and 4, are rejected under 35 U.S.C. 103(a) as being unpatentable over Horie in view of Zhao and in further view of Pan et al. US patent No. 6,284,581.

Regarding claim 3, Horie and Zhao teach substantially the entire process step of claim 1 above. Horie further teaches the emitter material includes the first impurity and creating an emitter diffusion region 28 in the base below the emitter 36.

Horie and Zhao neither one teach explicitly the method of claim 2 further comprising annealing the vertical bipolar transistor to drive the first impurity into the base to create an emitter diffusion region in the base below each emitter.

Pan teaches annealing the vertical transistor to drive impurities into the base to create an emitter diffusion region EM in the base below the emitter (Pan, fig. 7).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the annealing process taught by Pan in the method by Horie and Zhao in order to speed the diffusion process.

Regarding claim 4, Horie and Zhao teach substantially the entire process step of claim 1 above including the method of claim 2 further comprising: patterning a second

mask 32 over the bipolar region the mask including openings through to the base layer between one of the emitter 36 (Horie, figs 3a-3g).

Horie and Zhao neither one teach explicitly implanting additional amounts of the second impurity into the base layer through the opening.

Pan teaches implanting impurity contact region B within the base region 17.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to implant impurity regions taught by Pan in the process of Horie and Zhao in order to reduce contact resistance between base region and base electrode.

Claims 6-9, 11-15 and 17, are rejected under 35 U.S.C. 103(a) as being unpatentable over Pan in view of Horie and in further view of Zhao.

Regarding claim 6, Pan teaches a method of forming CMOS devices and vertical bipolar transistor on an integrated circuit chip comprising: providing a substrate having a collector layer 13 and a base layer 17; forming a polysilicon region layer 18 over the CMOS region of the silicon substrate; pattering a mask 20 over the polysilicon layer and bipolar region of the silicon substrate, the mask including opening 20'over the bipolar region; forming the emitter; removing the mask; patterning the polysilicon layer to form gate conductors 18N and 18P and forming sidewall spacers SP adjacent the emitter and the gate conductors (figs. 1-13).

Pan does not teach providing a silicon over insulator (SOI) substrate and depositing emitter material in the openings in a damascene process to form more than one emitter.

Horie teaches using SOI structure including an insulator layer between a bottom silicon layer and a top silicon layer as a substrate and depositing emitter material in the opening.

Horie does not teach a damascene process to form emitter.

Zhao teaches the use of damascene process for forming inter-connect structure in dielectric layer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the SOI substrate taught by Horie in the process of Pan since SOI structures facilitate faster operating speeds. It would also have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate depositing emitter material taught by Horie since the method is widely known in the art as an alternative for forming device structures. It would also have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate using damascene process taught by Zhao in order to form the emitter of the bipolar transistor since damascene process provides process simplification by reducing process steps required to form vias (Zhao, column 1, lines 27-45). It would also have been obvious to one of ordinary skill in the art at the time the invention was made to make more than one opening and filling the openings in the mask with emitter material since the formation integrated circuit involves the fabrication of more than one bipolar transistor.

Regarding claim 7, Pan, Horie and Zhao teach substantially the entire process step of claim 6 above including implanting a first impurity to form the collector layer 13 in

a lower portion of the silicon layer and the insulator layer and implanting a second impurity to the base layer 17 in an upper portion of the top silicon layer (Pan, fig. 7).

Regarding claim 8, Pan, Horie and Zhao teach substantially the entire process step of claim 6 above including the emitter material includes the first impurity and the method further comprises annealing the vertical bipolar transistor to drive the first impurity into the base to create an emitter diffusion region EM in the base below the emitter (Pan, fig. 7).

Regarding claim 9, Pan, Horie and Zhao teach substantially the entire process step of claim 6 above including patterning a second mask MP over the bipolar region, the mask including second opening 30' through to the base layer adjacent one of the emitter and implanting additional amounts of the second impurity into the base layer through the openings (fig. 6).

Regarding claim 10, Pan, Horie and Zhao teach substantially the entire process step of claim 6 above including forming a protective layer CM over the emitter region and implanting additional amounts of the first impurity into the silicon layer to provide a collector contact region C (fig. 2).

Regarding claim 11, Pan, Horie and Zhao teach substantially the entire process step of claim 6 above including before forming of the polysilicon forming a gate oxide layer GOX over the CMOS region of the SOI substrate (fig. 3).

Regarding claims 12-15 and 17, Pan, Horie and Zhao teach substantially the entire process step of claims 1-4, 6-9 and 11 above including pattering a mask 30 and

forming a gate conductor material; removing the mask; and forming sidewall spacers SP adjacent the emitter and gate conductors 18N and 18P (figs. 1-13).

Pan does not teach depositing a gate conductor material in the opening.

Horie teaches depositing emitter material in the opening.

It would have been obvious to one of ordinary skill in the art at the time the invention was made depositing gate material instead of emitter material as taught by Horie since the method is widely known in the art as an alternative for forming device structures.

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References D-F are cited as being related to BICMOS process.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel Admassu Gebremariam whose telephone number is 703 305 1913. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Samuel Admassu Gebremariam
April 18, 2002

Steven Loke
Primary Examiner